Centre Tecnològic de Telecomunicacions de Catalunya

Agile and high-performance SDR systems

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Team members: Pepe Rubio

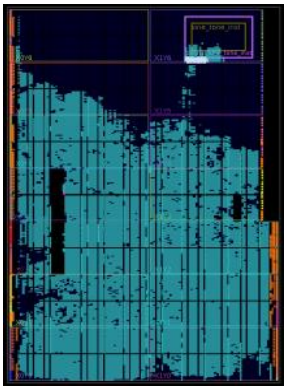
Programming languages & design tools:

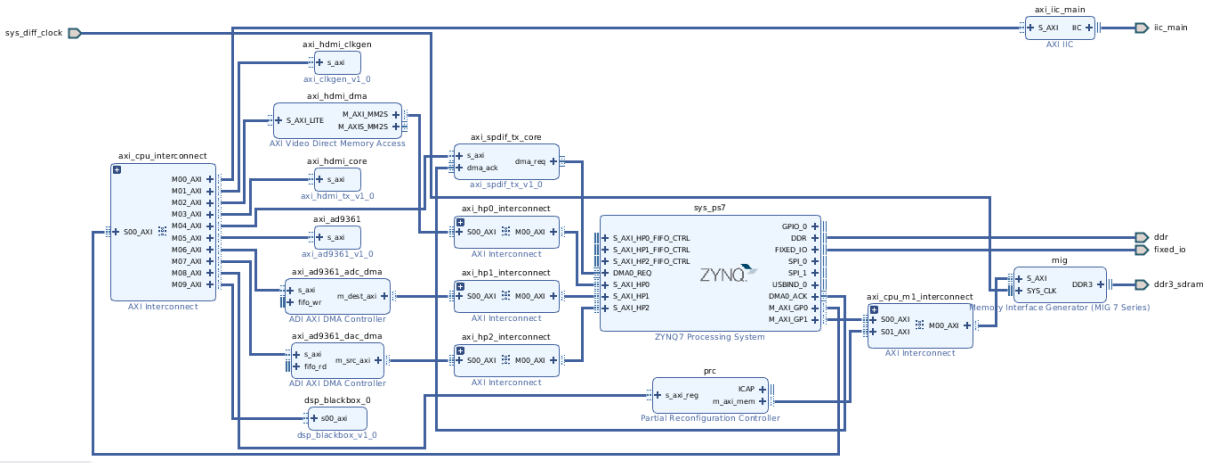
- **System/Algorithm modelling:** Matlab
- **SDR programming** (targeting general-purpose processors): C/C++,
- **HDL coding**: VHDL, Verilog
- **Embedded OS:** Xilinx PetaLinux, Analog Devices Ubuntu distribution
- **Embedded MPSoC tools:** Xilinx Open Asymmetric Multi Processing (OpenAMP)
- **FPGA design tools:** Mentor Questasim, Xilinx Vivado toolchain
- **SDR frameworks:** GNU Radio (with RFNoC)
- **Use/Integration of 3rd party code:** ns-3 LTE extensions (LENA)
- **FPGA devices (Xilinx):** Virtex 7, Kintex 7, Xilinx Zynq-7000, Zynq UltraScale+ MPSoC
- **Design methodology, COTS SDR platforms & developed demonstrators:** see the related sections in GEDOMIS®

This research topic comprises **four areas** featuring a certain degree of interdependency and complementarity among them**.** In the following, we are summarizing the key facts and figures of **each focused area** (i.e., ordered according to their **maturity level**).

Focused R&D area 1

- PHY-layer **digital design** for **SDR** systems that require **real-time FPGA co-processing** in order to accelerate bit-intensive DSP algorithms.
- **Hardware-software co-design** applied to FPGA-based SoC devices.
- Run-time **partial reconfiguration** of HDL and firmware functions targeting the programmable logic (PL) and processing system (PS) respectively of FPGA-based SoC devices.





Partial reconfiguration solution for a Zynq-7000 device (click to enlarge the figure).

Related projects

- **Ongoing**
  - **National**: ORIGIN, SensorQ (MoD)
- **Previous:**
  - **H2020:** Flex5Gware, ORCA (third party)
  - **FP7:** BeFEMTO, BuNGee, Emphatic
  - **National/regional**: 5G-TRIDENT, AEThER, GRE3N, GEDOMIS-ADCOMM, MIMOWA
  - **Industrial:** AT4 Wireless (Keysight, USA), ITERATE (TTI Norte, Spain), BeMImoMAX (Nutaq, Canada), GIPRE, (Gilat, Israel), Small Cell AVE (Hispasat, Spain)

Key developed technologies: FPGA-based SDR making use of the GEDOMIS® testbed

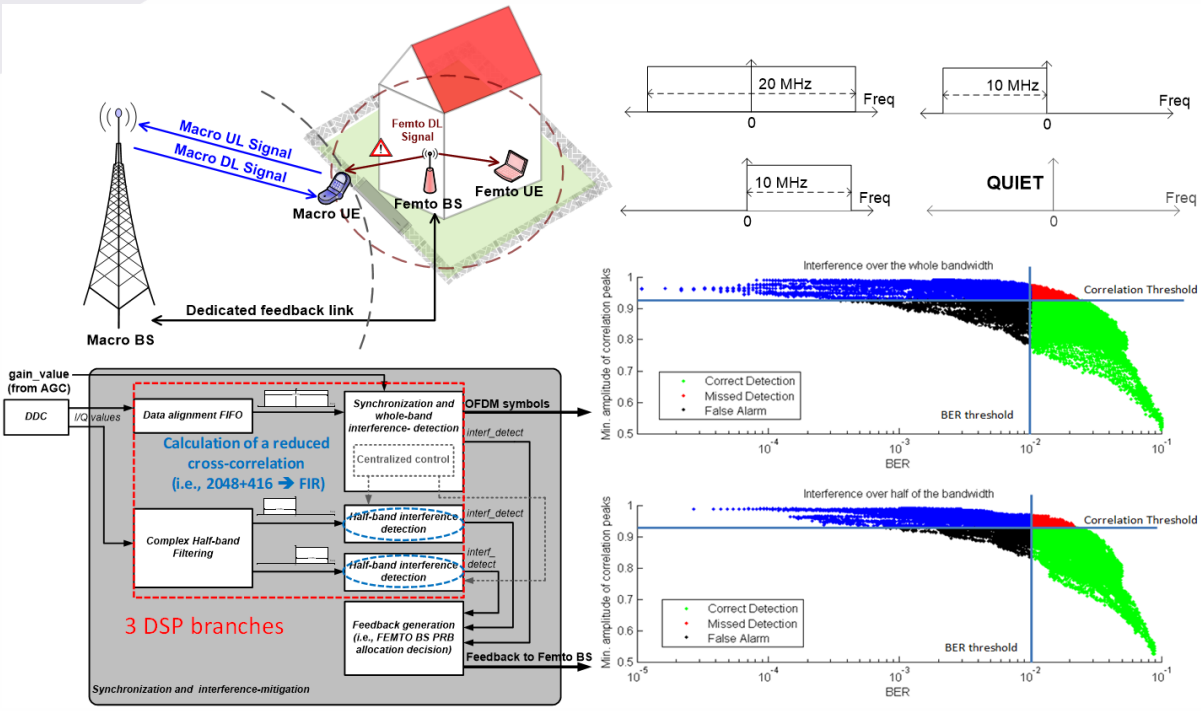
- PHY-layer of mobile WiMAX and **LTE rel. 9, 10 (eNB & UE)** featuring different **MIMO schemes**.
  - Selected references: [1], [2], [3]
  - Tutorial, IC1004/Newcom# School, Castelldefels, Spain, November 2013
- **Interference mitigation** in Heterogeneous Networks using **cognitive radio** principles.
  - Selected references: [1], [2], [3]
  - Tutorial, Newcom# Summer School, Sophia-Antipolis, France, May 2013
- Flexible **spectral coexistence** of broadband **FBMC** or LTE waveforms with primary narrowband transmissions (TETRA/TETRAPOL).
  - Selected references: [1], [2], [3]
  - Tutorial, Newcom# Spring School, Rennes, France, May 2014
- Digital Front End (DFE) and system interfacing of a **5G multi-antenna Remote Radio Head (RRH)**.
  - Contact us for more information
- Run-time **partial reconfiguration** of FPGA-based SDR platforms for 5G use cases.
  - Dissemination in progress

Ongoing R&D effort

- 5G NR
- NB-IoT

Focused R&D area 2

- Design of **DSP algorithms** for wireless communication systems



Design of a joint synchronization and interference mitigation algorithm: the LTE DL signal received by a UE (served by a macro BS) receives also the interfering DL signal of a femto HeNB operating in the same band (click to enlarge).

Related projects

- **Ongoing:**
  - **National**: 5G-TRIDENT, SensorQ (MoD)
- **Previous:**
  - **EC- funded projects:** CoopCom (FET), BeFEMTO (FP7), Emphatic (FP7)

- **Industrial:** AT4 Wireless (Keysight, USA), MUMO (Dimat ZIV, Spain), Small Cell Ave (Hispasat, Spain), MBIESA (MBI, Italy), SatNEx (European Space Agency), Inmarsat-I6 (Inmarsat, UK), I-CUBE (Inmarsat, UK).
- **Internal:** SiLenCe

Key developed technologies: some of which used the GEDOMIS® testbed

- Wireless **synchronization** for **5G NR** and 4G.
- **Modelling of 5G NR** and **LTE** Physical layer standard and development of a real-time **4G-LTE standard-compliant platform** to test user equipment.
- Design of **interference management algorithms** for macrocell/femtocell coordination in 4G-LTE.
- Development of new algorithms and implementation of **cooperative schemes for wireless relay networks**.
- Design and Implementation of an integral communications system for **HV-PLC (High Voltage - Power Line Communications)**.
- Design of novel **energy-harvesting-aware transmission policies** for ultra-low power mMTC.
- Design and implementation of **spectrum sensing algorithms** in the context of Broadband Professional Mobile Radio based on compressed sensing.

Ongoing R&D effort

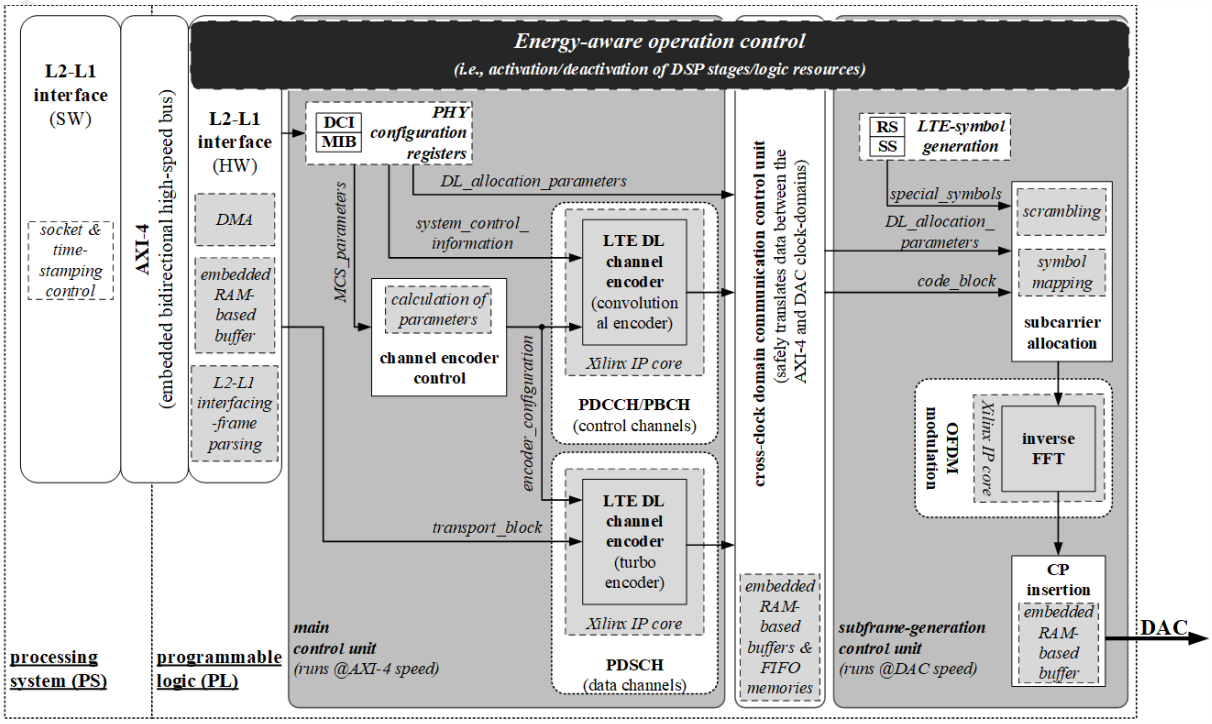
- 5G NR
- NB-IoT

Key references

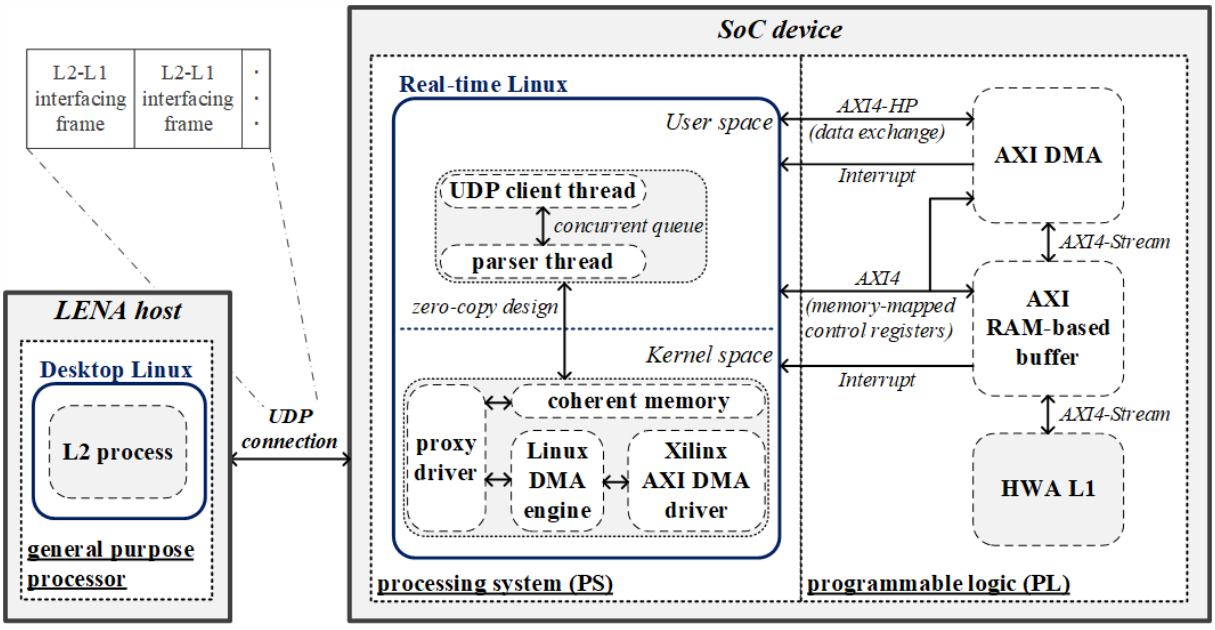
- Interference Management in LTE-based HetNets: a Practical Approach.
- Sparse Multiple Relay Selection for Network Beamforming with Individual Power Constraints Using Semidefinite Relaxation.
- Feasibility of Energy Management Techniques for Ultra-low Power M2M SatCom Terminals.

Focused R&D Area 3

- Design, implementation and KPI-driven validation of **flexible SDR** systems serving **RAN functional splits (FS)**



HW-SW codesign using a Zynq-7000 for the functional split 6 at the eNB side.



MAC-PHY interface for an uninterrupted real-time operation.

Related projects

- **Ongoing:**
  - 5G-TRIDENT
- **Previous:**
  - **H2020:** Flex5Gware
  - **National**: AEThER

Key developed technologies: FPGA-based SDR making use of the GEDOMIS® testbed

- Integration of a proprietary **FPGA-based real-time PHY-layer** with the **MAC-layer of LENA** (LTE extensions of ns-3), through a flexible **PHY-MAC interface** using a COTS SDR platform.
- Functional split 6 (**PHY-MAC**) and 8 (**PHY-RF**) as defined in the 3GPP standard.

Key references:

- [1], [2], [3], [4]

Talks:

- Partitioning and distributing communication stack functions of 5G wireless hotspots, EuCNC 2016, 5GPPP Workshop on 5G Physical Layer Design and Hardware Aspects Below and Above 6 GHz, 27 June 2016, Athens, Greece.
- Extending the ns-3 LTE module for SDR:a HW-SW function split paradigm, CrownCom 2018, Open radio platforms workshop, 19 September 2018, Ghent, Belgium

Ongoing R&D effort

- KPI-driven dynamic FS reconfiguration

Focused R&D area 4

- Design and integration of **hardware-accelerated functions** in the context of **NFV** and **adaptive SDR** end-scenarios

Related work/projects

- Ongoing effort

Key references

- Relevant publications in the literature (to be added)