Centre Tecnològic de
Telecomunicacions de Catalunya

GEDOMIS® testbed

GEDOMIS® GEneric DemOnstrator for Modular and aglle SDR Systems

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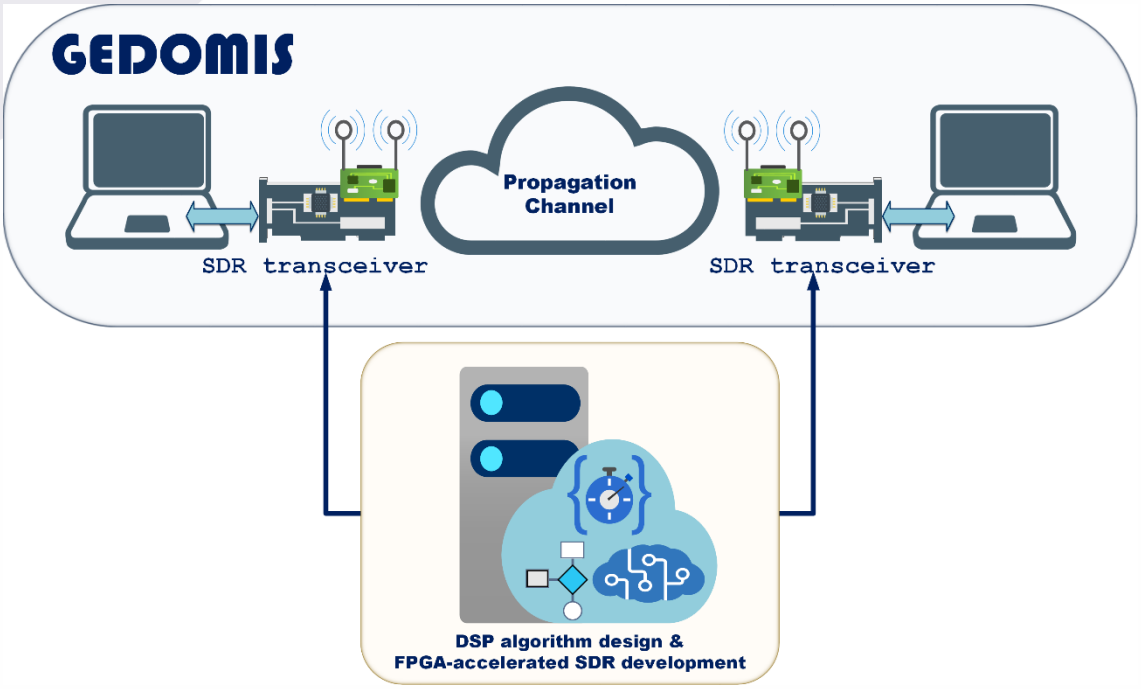
1. GEDOMIS® in a nutshell

GEneric Dem**O**nstrator for **M**odular and ag**I**le SDR **S**ystems -**GEDOMIS®**- is a highly **customizable testbed** comprising a number of **software defined radio (SDR) platforms**, which can be used to develop 5G and beyond **wireless communication** systems, targeting **below 6 GHz** applications. In addition, GEDOMIS® includes a **real-time multi-channel channel emulator** and other **test & measurement (T&M) equipment** to facilitate the validation and testing of realistic radio communications scenarios, before conducting field trials. The hardware and software building blocks of GEDOMIS® can be configured, customized and programmed according to different prototyping or experimental needs.



Starting from 2009, GEDOMIS® has been used to prototype a number of real-time demonstrators. The most complex development carried out in GEDOMIS®, was a **propriety implementation of the DL LTE PHY-layer**, which was **interfaced with** a purpose-built customization of CTTC's EXTREME® testbed. The latter hosted a suitably modified version of the ns-3 LTE extensions (LENA). The interfacing of the two testbeds and the key modifications applied to LENA were the following: **i)** the single software process of LENA was divided in three separate processes (i.e., for the eNB, UE and EPC), **ii)** the abstracted PHY-layer of LENA was substituted with the one developed in GEDOMIS® and **iii)** the two testbeds were connected through a custom PHY-MAC interface, which guaranteed uninterrupted real-time connectivity between the two layers. This joint **end-to-end real-time testbed** added **over-the-air** testing capabilities to LENA and helped to validate different **RAN functional splits** and **KPIs**.

2. SDR platforms

The following SDR platforms have been used in different setups of the GEDOMIS® testbed:

- The **Xilinx ZC706 Evaluation Kit** fitted with a Xilinx Zynq-7000 device and interfaced through the FMC slot with the **Analog Devices AD-FMCOMMS-3** evaluation board (**figure 1.a**). The latter features the AD9361 2x2 RF transceiver IC (TX band: 47 MHz to 6.0 GHz, RX band: 70 MHz to 6.0 GHz, tunable channel bandwidth: 200 kHz to 56 MHz). In total GEDOMIS® disposes **five** Xilinx ZC706 boards and **five** AD-FMCOMMS-3 RF front-ends.
- The **Xilinx ZCU102 Evaluation Kit** fitted with a Zynq UltraScale+ MPSoC device (**figure 1.c**) and interfaced through the FMC slot with the **Analog Devices AD-FMCDAQ2** evaluation board (**figure 1.b**). The latter comprises the AD9680 ADC (dual 14-bit, 1.0 GSPS, JESD204B) and the AD9144 DAC (quad 16-bit, 2.8 GSPS, JESD204B). The Xilinx ZCU102 was also combined with the AD-FMCOMMS-3 evaluation board.
- The **Ettus Research USRP X310** SDR board, also commercialized as **NI USRP-2943R**, which includes an agile RF transceiver module able to be programmed for a large range of RF frequencies (from 1.2 GHz to 6 GHZ, channel bandwidth 40 MHz) and a Xilinx Kintex-7 FPGA device.
- The **Ettus Research USRP N210** board (**figure 1.d**) featuring a Xilinx Spartan 3A-DSP 3400 FPGA, a dual ADC (100 MS/s), a dual DAC (400 MS/s) and GigE connectivity to stream data to and from host processors.
- GEDOMIS® has also made use of other FPGA-based SDR prototyping boards such as the **Xilinx VC707 Evaluation Kit** (featuring a Xilinx Virtex 7 device), the **Xilinx KC705 Evaluation board** (featuring a Xilinx Kintex-7 device) and the **Xilinx Zedboard** (featuring a small Zynq-7000 device), which can be combined with the above mentioned RF front-ends of Analog Devices.

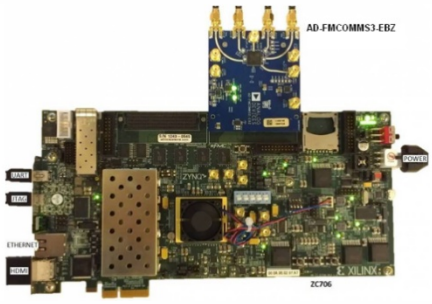


Figure 1.a: The Xilinx ZC706 board with the AD-FCOMMS-3 RF front-end.

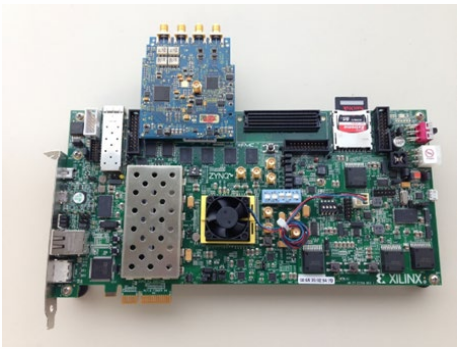


Figure 1.b: The Xilinx ZC706 board with the AD-FMCDAQ2.

Figure 1.c: The Xilinx ZCU102 board.

Figure 1.d: The USRP N210.

Outphased SDR platforms

- The **Nutaq uSDR420** platform, with a Virtex-6 SX475T device, frequency range of 0.3–3.0 GHz, selectable bandwidth (1.5–28.0 MHz) and able to host 2x2 MIMO systems.
- The **Lyrtech ADP** platform combined with two **Agilent E4438C** VSGs (RF up-conversion) & the Mercury Computer Systems **RF 3000T** (4 channels phase-coherent RF down-conversion)**.** The Lyrtech ADP is a modular platform featuring:
  - 1 cPCI board with 8 A\D channels (14 bit, 105 MSPS) and a Virtex-4 FPGA device,
  - 1 cPCI board with 8 D\A channels (14 bit, 480 MSPS) and a Virtex-4 FPGA device,
  - 1 cPCI board featuring 2 Virtex-4 FPGA devices and two extra mezzanine boards featuring 2 more Virtex-4 FPGA devices.
  - 1 cPCI board featuring an embedded PC used to control & program the other boards through proprietary APIs.
  - The ADC and DAC boards are interconnected with the main FPGA board through a proprietary high-speed bus interface.
  - A chassis with a cPCI backplane hosts all the previous boards.

3. Test & measurements

Radio Channel Propagation

GEDOMIS® makes use of the following options for the radio channel propagation:

- **Over-the-air** indoor transmissions
  - Unlicensed bands (under controlled conditions)
- **RF shielded test enclosures** for device/component validation e.g., similar to this one
  - Interference-free testing and validation in licensed/unlicensed bands
- **Anechoic chamber**
  - Wireless communication devices measurements. More info here.
- **Elektrobit (EB) C8 multi-channel emulator**
  - Below 6 GHz real-time multi-channel emulation

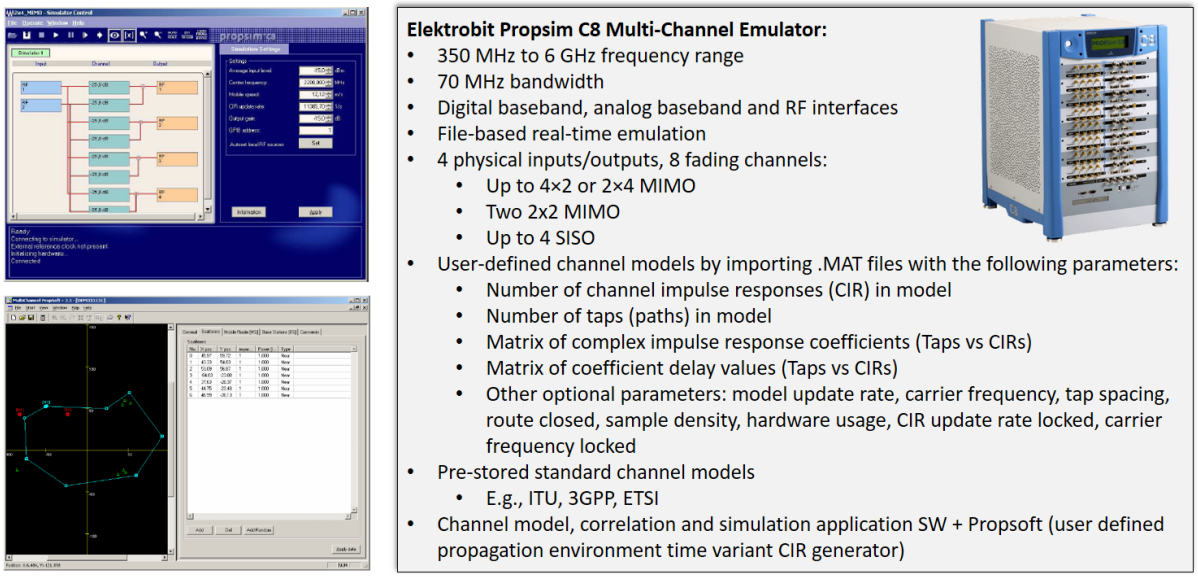


Figure 2. Main specifications of the C8 Multi-Channel Emulator and indicative control software captures.

The channel emulator is a critical asset of GEDOMIS®, since it allows testing the effects of channel propagation of radio systems before embarking to field measurement campaigns. The instrument allows performing **realistic and accurate radio channel emulation**, where the physical radio channel characteristics, such as frequency, multipath propagation, fast fading, dynamic delays, attenuation and shadowing can be emulated independently on each channel. The EB Propsim C8 provides channel modelling tools to create custom channel models and modify pre-defined standard channel models. In addition to statistical and spatial channel models, measured channel data or data collected with various measurement tools can also be used. Key specifications of this instrument are provided in **figure 2**.

Other T&M instruments

GEDOMIS® also disposes a number of other instruments that could be employed at an early stage of testing, validation and SDR prototyping:

- **Agilent E4438C ESG vector signal generators (VSG)** delivering calibrated test signals at baseband, IF, and RF frequencies up to 6 GHz. By using two or more VSGs, MIMO transmission could be enabled too.
- **Applied Instruments NS3 AWGN generation** units (from 5 MHz to 2.15 GHz).
- **Holzworth HS1001A & HSM1001A RF Synthesizers** used for high-precision clock generation and RF synthesis.
- **Rohde Schwarz FSQ26** spectrum analyzer (up to 26.5 GHz).
- **Agilent Infiniium DSO80804B** multi-channel oscilloscope (4 channels, 8 GHz analog bandwidth, up to 40 GSPS). The latter can be combined with the **Keysight VSA 89600** (full academic license) software to demodulate different wireless standards of interest.

4. Prototyping methodology

Real-time SDR systems

- The majority of the SDR proof-of-concepts (PoC) and experimental work conducted with GEDOMIS® in the past, were based on FPGA-based **hardware-accelerated baseband systems operating in real-time**. This implied the development of custom **HDL code (VHDL, Verilog)** targeting the FPGA devices of different SDR platforms. In the case of FPGA-based SoC devices, such as the Xilinx Zynq-7000 and Zynq UltraScale+ MPSoC, a HW-SW co-design approach was followed.

SDR systems operating offline

- GEDOMIS® has also been used in many other occasions for testing and validation campaigns of system operating in **offline mode**. The latter implied **waveform playback and waveform recording** at the transmit and receive ends respectively and **offline post-processing** of the captured data sets in a host computer (in Matlab). The offline validation of developed algorithms or parts of the baseband system also forms part of the early testing (rapid prototyping) conducted during real-time system design.

Development flow

GEDOMIS® is used throughout the SDR development cycle, from early algorithm exploration up to a system-wide validation and KPI-driven measurement campaign. Thanks to the modularity and flexibility of its underlying hardware and software components, the testbed can be **customized for a given operating scenario**. The **programming languages** and **design tools** used for the SDR development flow are listed here. An example of the **FPGA-based SDR development flow** is given next:

- **Preliminary/feasibility analysis stage:**
  - Analyze specifications, requirements, constraints & use cases.
  - Conceptual design (e.g., baseband building blocks & required I/O interfacing).
  - Selection of DSP algorithms & early estimation of their computational complexity.
  - Selection of SDR platform (already existing or acquisition of a new COTS):
    - RF front-end & signal converters (modular solution): RF up and down converter chains, ADC & DAC devices (e.g., packed in a zero-IF RFIC).
    - RF filters and PA (whenever it applies).
    - Baseband processing solution (e.g., FPGA device family).
    - Required I/O interfaces & protocols (e.g., 10GigE, CPRI).
- **System/algorithm design:**
  - High-level modular design in Matlab of the DSP algorithms and system.
  - Modifying the previous Matlab design to provide a cycle-accurate & hardware-aware system model.
  - Creation of test vectors in Matlab to facilitate incremental system validation (see next point).
  - Early evaluation of algorithms with GEDOMIS® boards/T&M instruments.
- **SDR baseband development:**
  - FPGA design (VHDL, Verilog, Simulink with System Generator).
  - HW-SW co-design targeting FPGA-based SoCs (HDL, C/C++).
  - Co-simulation of the cycle-accurate Matlab model versus HDL/C code.
- **Board-level code integration & interfacing of the DSP system/algorithm:**
  - Write/modify FPGA firmware to interface the developed baseband system with ADC, DAC and RFIC devices (e.g., through JESD204B, SerDes).

- Develop custom I/O interfacing or reuse standard protocols (CPRI, GigE, USB, PCIe) to connect the developed DSP system with other boards or devices.
- Tackle clock distribution issues (e.g., PLL programming, jitter cleaning).
- Synchronize multiple baseband processing boards & RF-front-ends.
- Mitigate signal impairments (e.g., I/Q imbalances, LO leakage, DC offset).
- Develop waveform-specific algorithms to interface with on-board components (e.g., Automatic Gain Control).

- **Experimental validation:**
  - Use signal generation, signal analysis and signal emulation instruments.
  - Measurement campaign according to defined scenarios, use cases & KPIs.

Another design flow serving **offline DSP system prototyping** purposes is shown in **figure 3**.

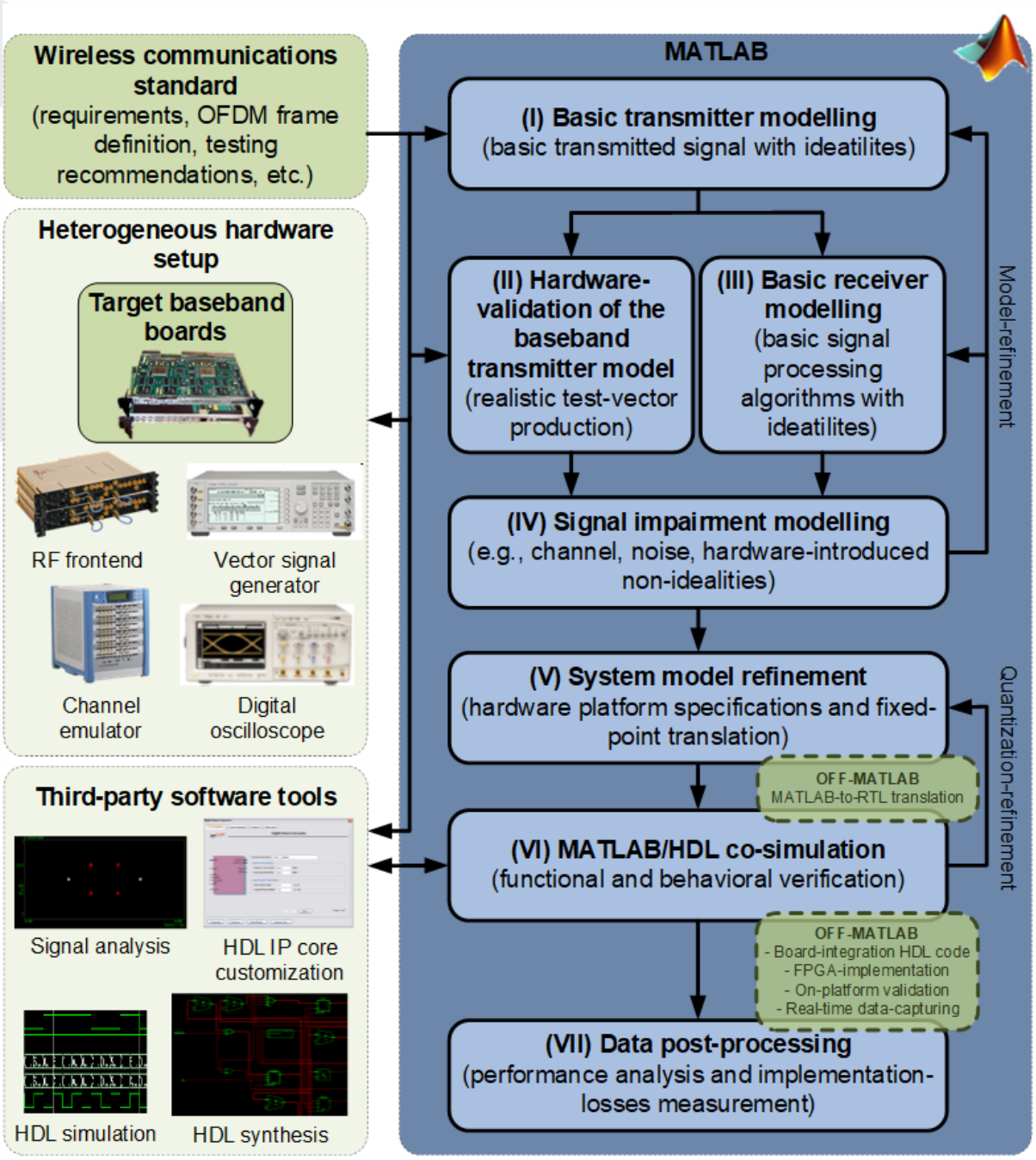


Figure 3: Offline prototyping methodology.

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5. Developed PoCs

Timeline

2019

- **Topic:** Run-time **partial reconfiguration** of programmable logic (PL) functions and processing system (PS) firmware developed for **agile SDR systems** featuring **FPGAs** and **FPGA MPSoCs** devices as hardware accelerators.
- **Projects:** ORCA (H2020, third party subcontracted by Imec under project ReproRun), 5G-TRIDENT (national).
- **SDR platforms:** **i)** Xilinx ZC706 Evaluation Kit combined with the Analog Devices AD-FMCOMMS-3 evaluation board, **ii)** Ettus Research USRP X310 platform.
- **Background:**
  - References: to be added soon.
  - VIDEO: to be added soon.
  - Figure 4.

2018

- **Topic:** Implementation of the **digital front-end functions** (crest factor reduction and digital predistortion) for multi-antenna **5G remote radio heads**, generating and looping back CPRI traffic on the same board.
- **Project:** ITERATE (industrial, TTI, Spain).
- **SDR platform:** Xilinx ZCU102 Evaluation Kit combined with the Analog Devices AD-FMCDAQ2 evaluation board.
- **Background:**
  - No further information can be disclosed.

2017

- **Topic:** Propriety implementation of the DL LTE PHY-layer, which was **integrated with** a purpose-built customization of CTTC's EXTREME® testbed. The latter hosted a suitably modified version of the ns-3 LTE extensions (LENA) (e.g., without LENA's native PHY-layer, adding a custom PHY-MAC interface, separating the software processes of the eNB, UE and EPC). This **joint end-to-end testbed** added **over-the-air** testing capabilities to LENA and helped to validate among others the PHY-MAC and PHY-RF **RAN functional splits** (FS 6 and FS 8 respectively) and also a number of different **KPIs**.
- **Projects:** Flex5Gware (H2020), AEThER (national).
- **SDR platform:** Xilinx ZC706 Evaluation Kit combined with the Analog Devices AD-FMCOMMS-3 evaluation board.
- **Background:**
  - References: [1], [2], [3].
  - Invited talk: CrownCom 2018 (Open radio Platforms Workshop).
  - VIDEO.
  - Figure 5 and Figure 6.

2014-2016

- **Topic: Spectral coexistence** of a configurable LTE-like **FBMC broadband waveform** (contemplating a MIMO scheme) with in-band **narrowband TETRAPOL** transmissions at the 400 MHz band.
- **Projects:** EMPhAtiC (FP7), NEWCOM# (FP7).
- **SDR platform:** Xilinx ZC706 Evaluation Kit combined with the Analog Devices AD-FMCOMMS-3 evaluation board.
- **Background:**
  - References: [4], [5], [6].
  - Tutorial: Newcom# Spring School (2014).
  - VIDEO#1, VIDEO#2.
  - Figure 7, Figure 8 and Figure 9.

2012-2013

- **Topic: Interference mitigation** in heterogeneous networks. Real-time FPGA implementation of a Macro BS and UE pair (primary transmission) operating in the same band with a Femto eNB and UE pair (secondary transmission). The customization of GEDOMIS® included RF up and down conversion and different channels applied to the real-time channel emulator. The interference detection scheme made use of different sub-bands (i.e., the 20 MHz spectrum was divided in two 10 MHz bands).
- **Projects:** BeFEMTO (FP7), NEWCOM# (FP7), GRE3N (national).
- **SDR platform** (legacy)**:** Lyrtech ADP platform combined with two Agilent E4438C VSGs (RF up-conversion) & the Mercury Computer Systems RF 3000T (4 channels phase-coherent RF down-conversion).
- **Background:**
  - References: [7] (more to be added).
  - Tutorial: Newcom# Summer School (2013).
  - VIDEO (legacy PoC).
  - Figure 10.

2009-2012

- **Topics: WiMAX** and **LTE PHY-layer** real-time PoCs featuring **MIMO**, **SIMO** and **MISO** antenna configurations. The baseband processing was entirely implemented in FPGA devices.
- **Projects:** MIMOWA, (national, MEDEA+), BuNGee (FP7), GEDOMIS-ADCOMM (regional), BeMImoMAX (industrial, Lyrtech/Nutaq Inc., Canada).
- **SDR platforms** (legacy)**: i)** Lyrtech ADP platform combined with two Agilent E4438C VSGs (RF up-conversion) & the Mercury Computer Systems RF 3000T (4 channels phase-coherent RF down-conversion), **ii)** Nutaq uSDR420 platform.
- **Background:**
  - References: [8], [9], [10] (selected).
  - BeMimoMAX brochure**:** Legacy technology transfer activity, showcasing a real-time MIMO OFDM system during the MWC 2012 (remote demonstration).
  - VIDEO#1**,** VIDEO#2 (legacy PoC).
  - Figure 11 and Figure 12**:** Legacy demonstrations.

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Gallery: figures, block diagrams & photos

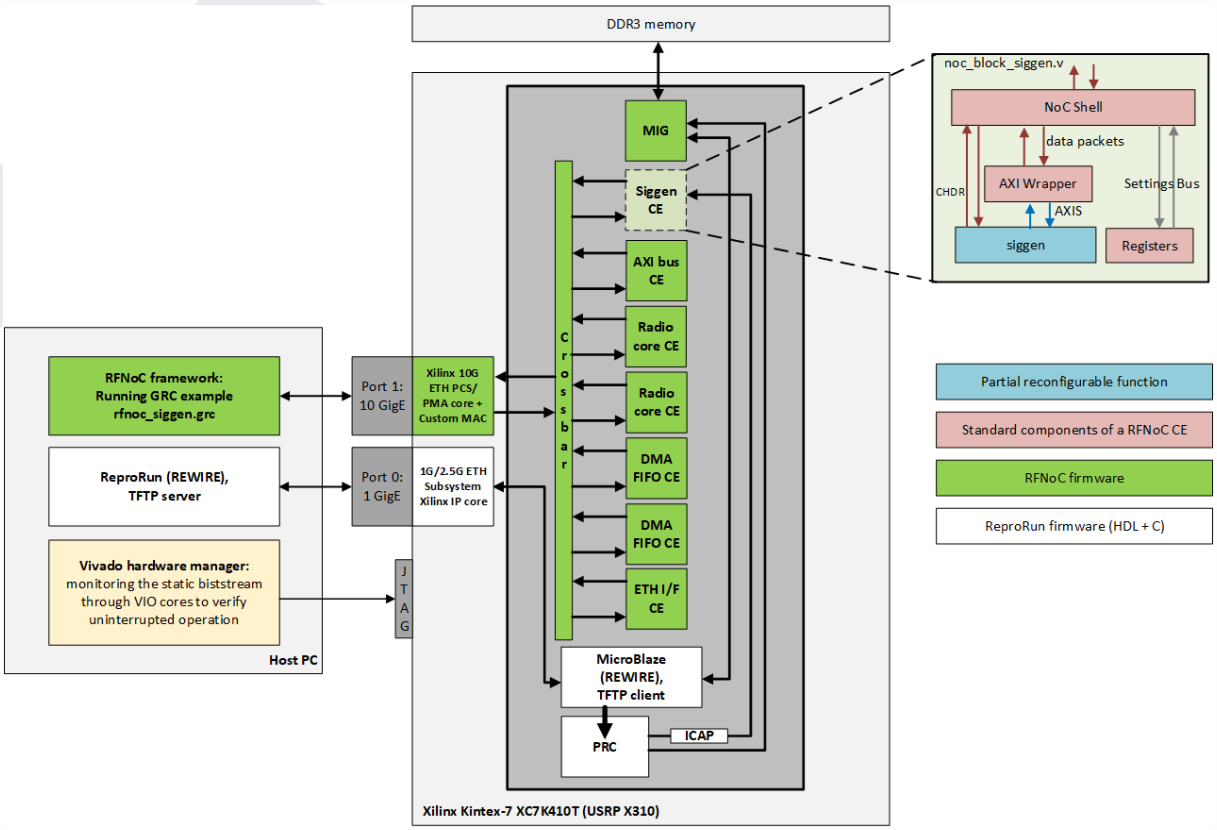

Figure 4: Run-time partial reconfiguration of PL-based DSP functions and PS-based firmware (both fetched through TFTP from a remote host), a concept that could be applied in NFV and other 5G key radio technologies. This PoC was developed in the framework of the H2020 ORCA project (ReproRun).

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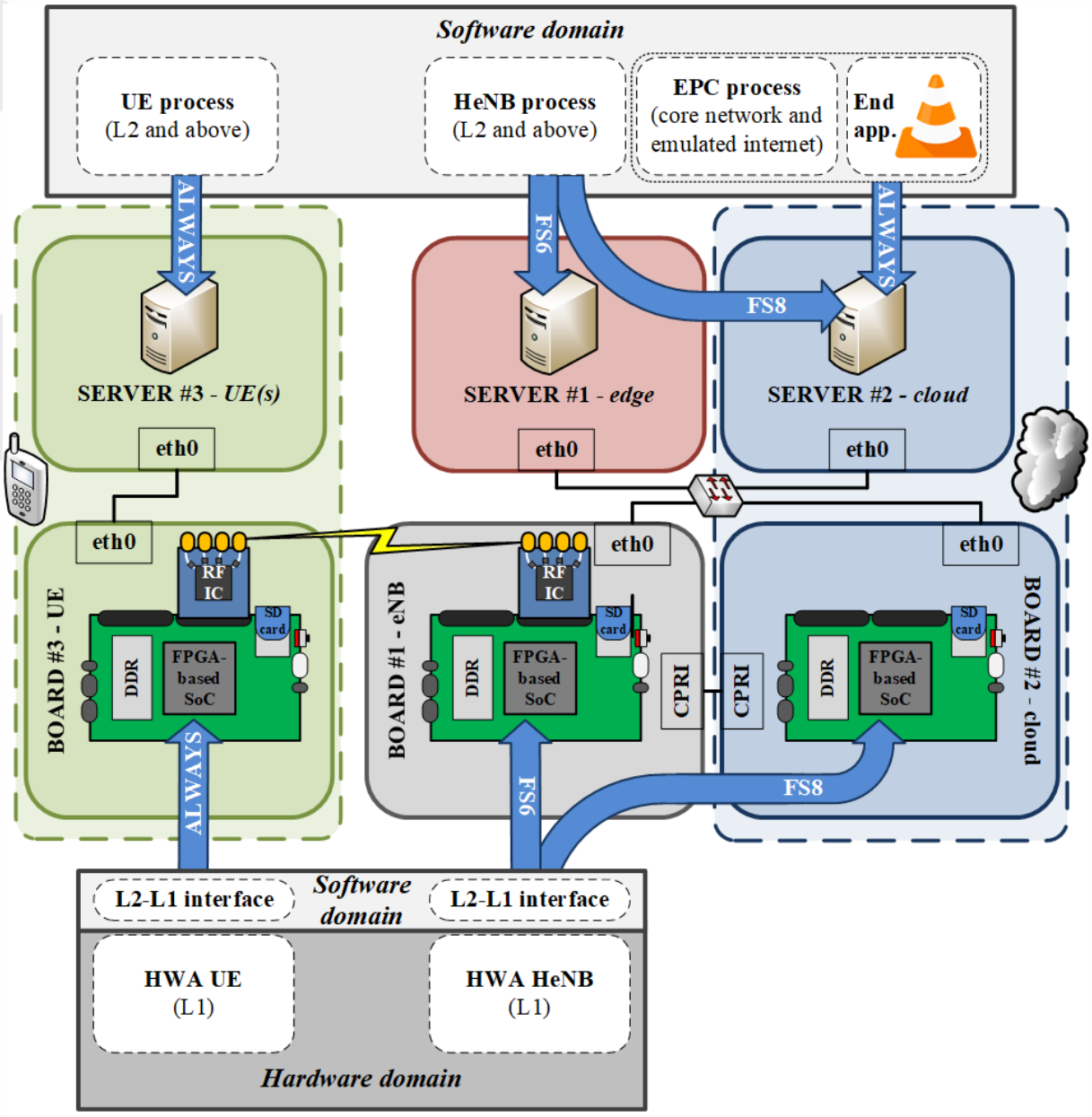

Figure 5: Functional Splits 6 (PHY-MAC) and 8 (PHY-RF) using a proprietary real-time FPGA implementation of the eNB and UE L1 and the ns-3 extensions for LTE (LENA) for the upper layers and EPC (project H2020 Flex5Gware).

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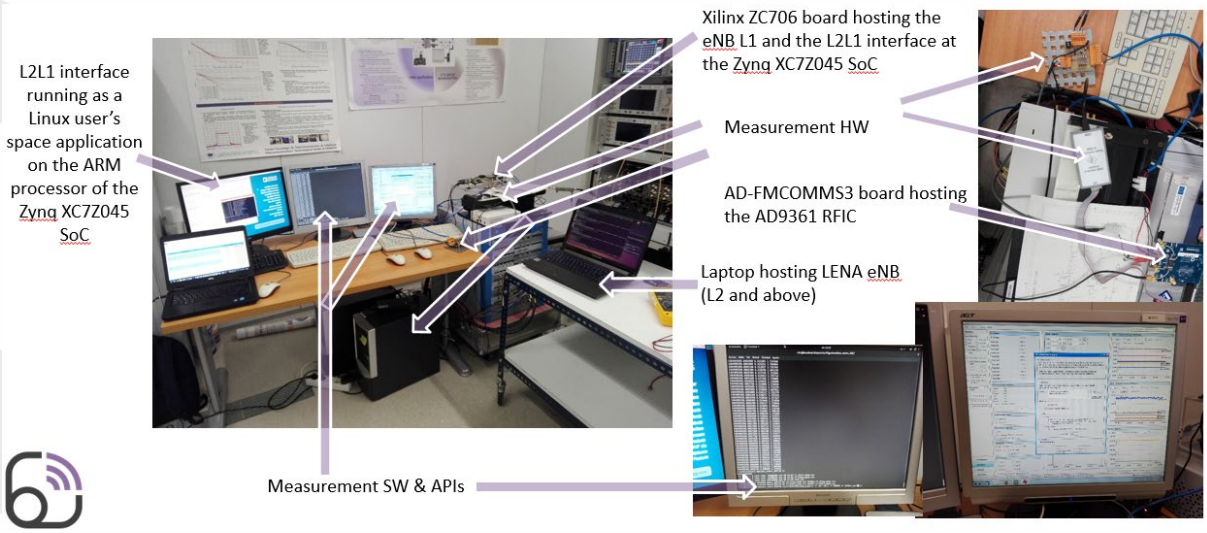

Figure 6: Measurement campaign for the Flex5Gware project in order to assess the energy consumption KPI in FPGA devices RF transceiver ICs and Ethernet ICs.

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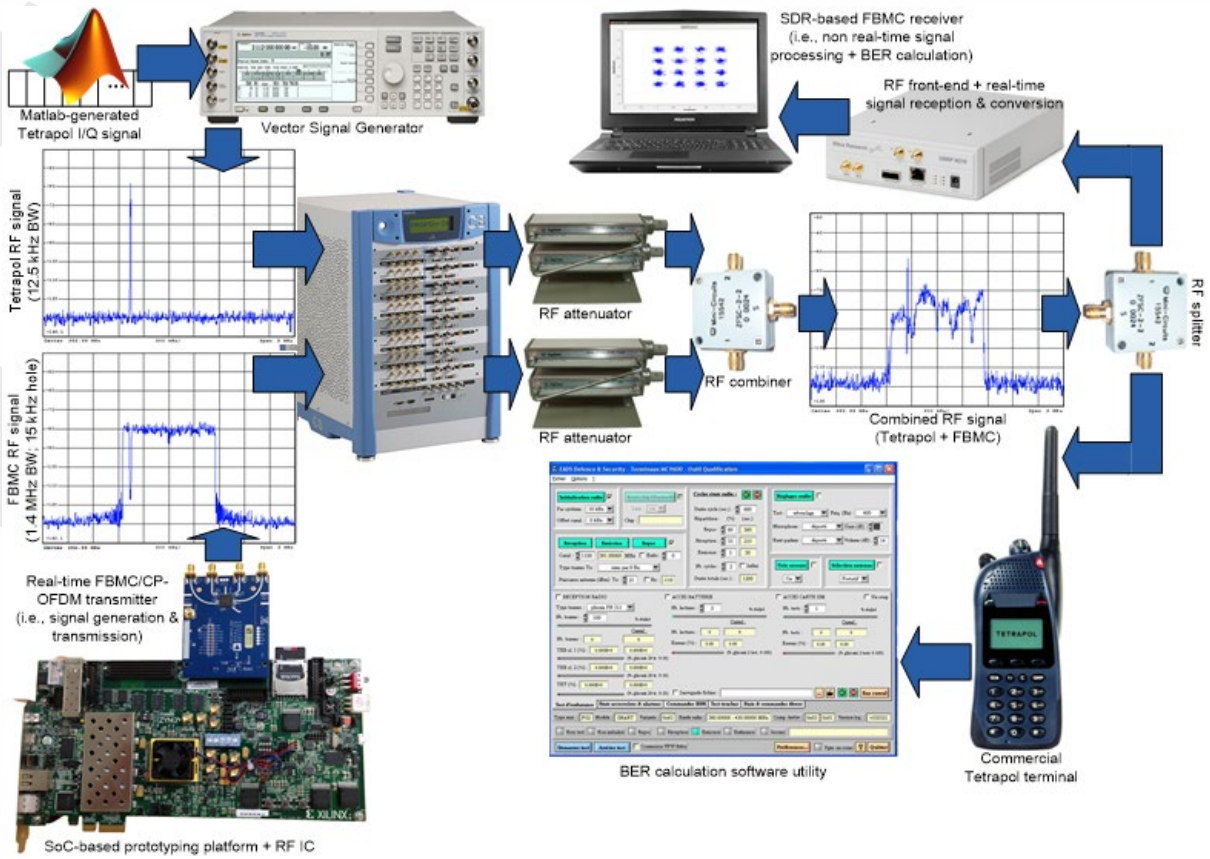

Figure 7: The setup of GEDOMIS® in the FP7 EMPhAtiC project. Flexible broadband FBMC transmitter (real-time FPGA implementation) coexisting with TETRAPOL transmissions at the 400 MHz band.

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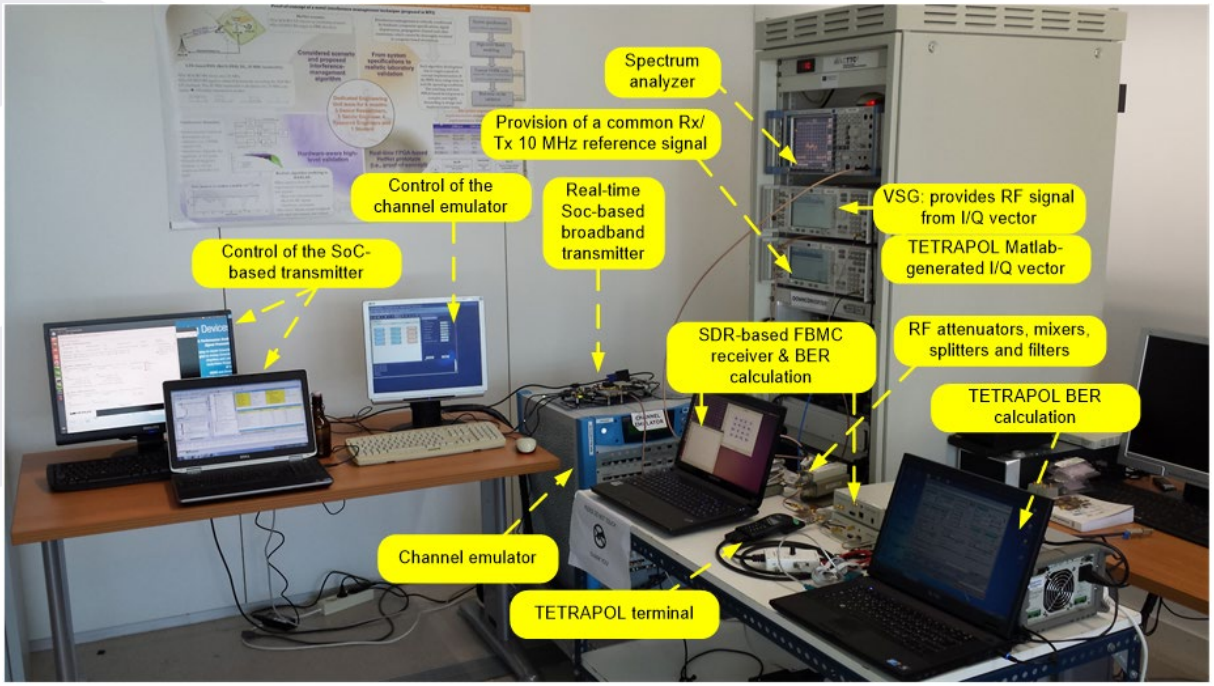

Figure 8: Flexible broadband FBMC transmitter (real-time FPGA implementation) coexisting with TETRAPOL transmissions at the 400 MHz band. Full PoC setup @CTTC.

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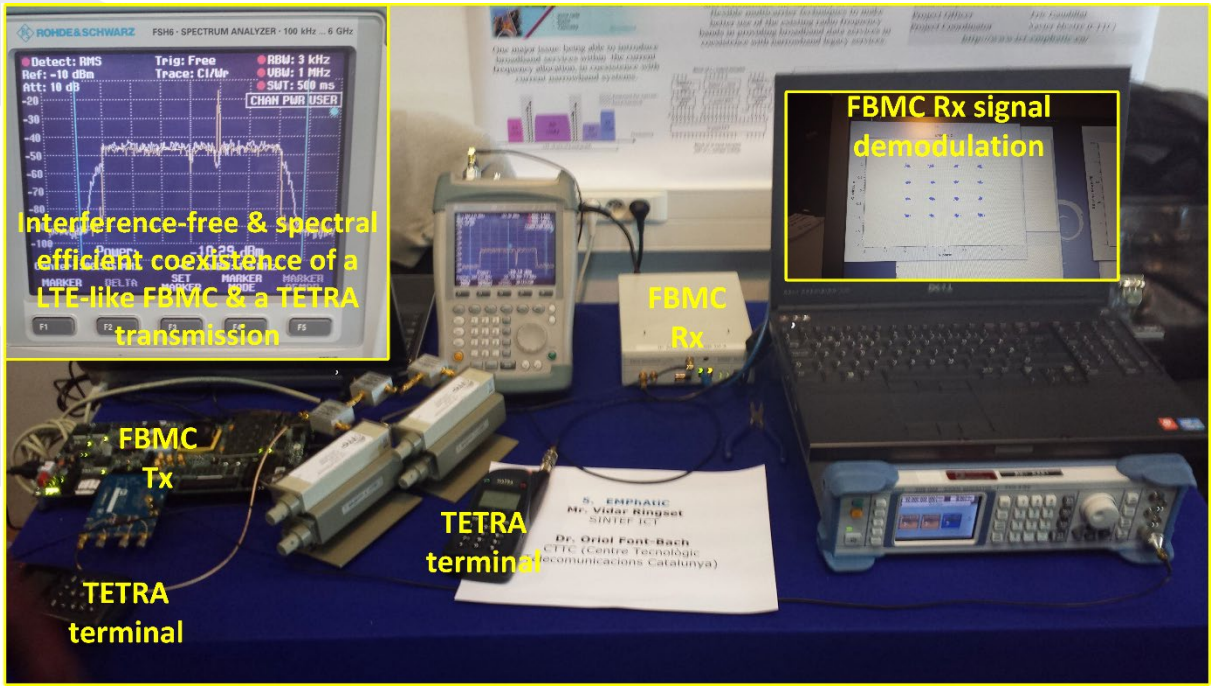

Figure 9: Flexible broadband FBMC transmitter (real-time FPGA implementation) coexisting with TETRA transmissions at the 400 MHz band. ETSI workshop on Reconfigurable Radio Systems, 3-4 December 2014, Sophia Antipolis, France.

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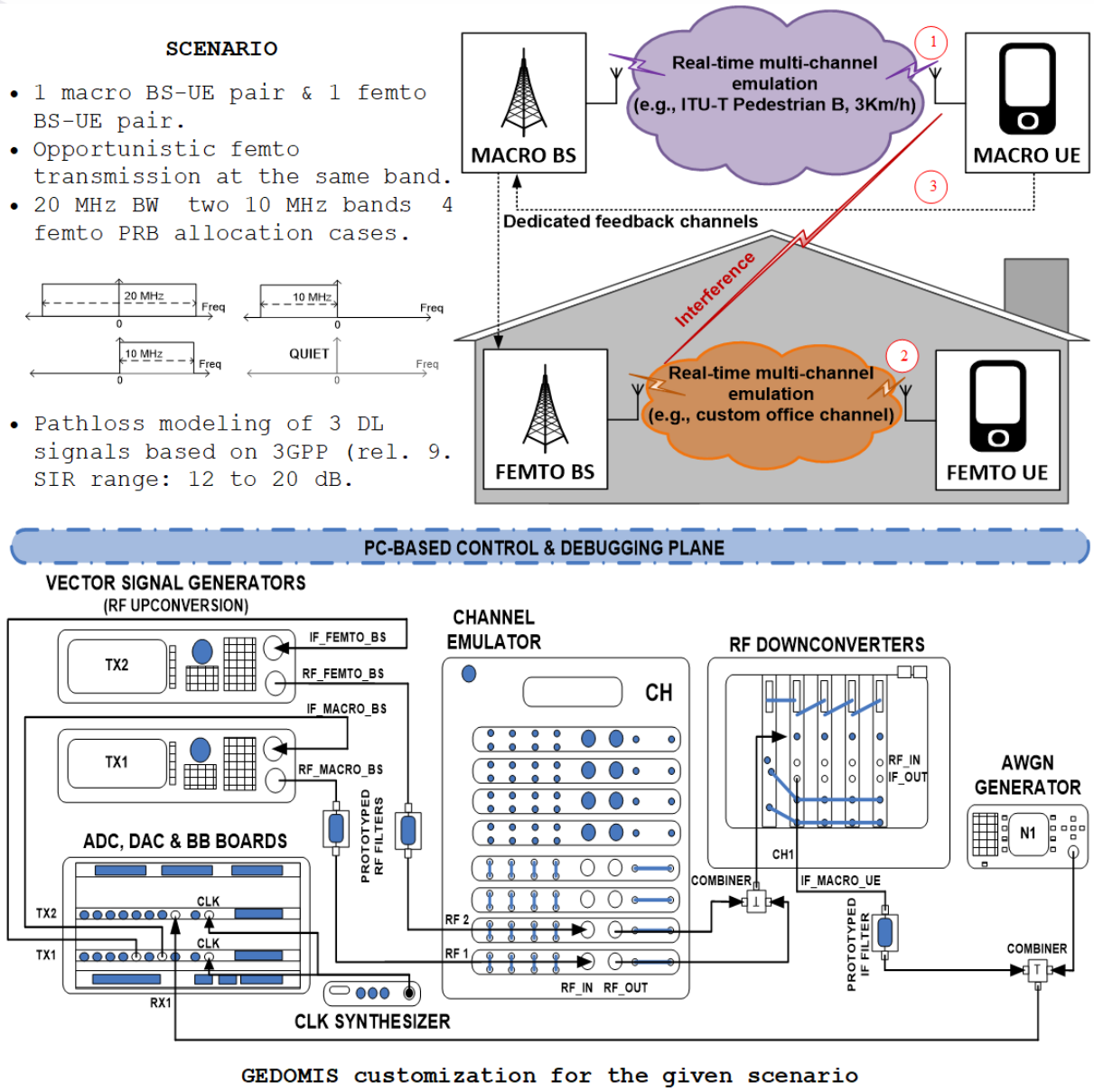

Figure 10: FPGA-based baseband system developed and experimentally validated using a GEDOMIS® SDR customization together and the real-time multi-channel emulator, in order demonstrate an interference mitigation scheme applied to HetNets.

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Figure 11: Demonstration of a 2x2 MIMO WiMAX Tx & Rx, real-time FPGA PHY implementation. European Nanoelectronics Forum 2010, Nov. 16-17, Madrid, Spain.

Figure 12: Remote access of the same demonstration. DSPecialists GmbH commercial event, 11-13 May 2011, Berlin, Germany.

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6. Next steps

Technologies planned to be developed using GEDOMIS®

- **PHY-layer** of a **NB-IoT** system targeting satellite communications.
- **5G NR PHY-layer** (ongoing effort) and interfacing with CTTC's 5G-LENA.
- **Hardware-accelerated NFV** framework for 5G and beyond systems.
- **ML techniques** for wireless communication systems (e.g., **figure 8**).

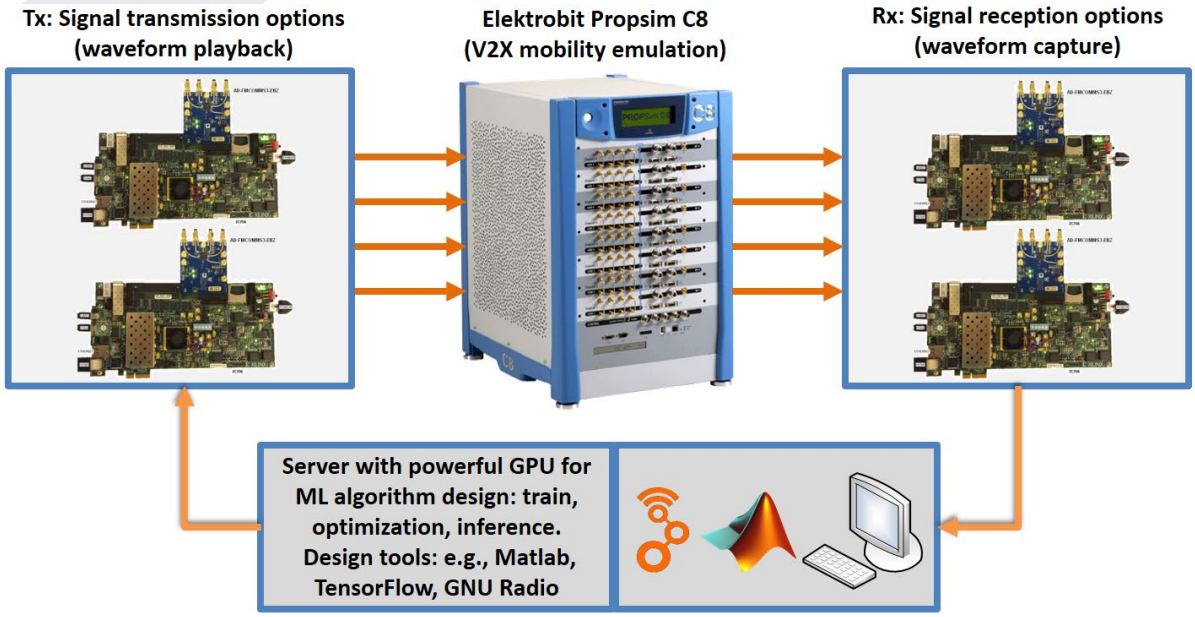

Figure 8: A potential customization of GEDOMIS® configured to operate in offline mode. This setup could serve the needs of a V2X scenario, helping to develop ML algorithms.

Forthcoming GEDOMIS® upgrades/extensions

- **Xilinx: Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit**
  - Development of a 5G gNB or RRH
- **Deepwave Digital: Artificial Intelligence Radio Transceiver (AIR-T)**
  - Machine learning extension for the GEDOMIS® testbed
- **Analog Devices: EVAL-ADRV9008/9 FMC evaluation kit**
  - Development of a 5G gNB or RRH
- **Rincon Research: AstroSDR**
  - Design CubeSat SDR-based payloads